
# RISC-V Instruction Set Architecture Update

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# RISC-V ISA Updates

- Leaving UC Berkeley
- ISA Extensions
- Memory Model
- Compressed Extension
- Vector Extension
- Privileged Spec v1.9
- External Debug Spec
- High Performance Monitor (HPM) counters
- Future Progress
- Ecosystem Updates

# RISC-V Timeline

- In summer of 2010, UC Berkeley started “3-month project” to develop their own clean-slate ISA
- May 2014, frozen user-level spec (IMAFDQ)
- August 2015, **non-profit RISC-V Foundation** created

# Transitioning RISC-V Out of UC Berkeley

- RISC-V Foundation is taking over standards process
  - Incorporated Aug 2015
  - Board of Directors formed Summer 2016
- Tools are starting the upstreaming process
- Students graduating
  - Lead RISC-V devs no longer at UCB
    - new start-up called SiFive
  - But many new students (github.com/ucb-bar)

# Foundation Mission Statement

*The RISC-V Foundation is a non-profit consortium chartered to standardize, protect, and promote the free and open RISC-V instruction set architecture together with its hardware and software ecosystem for use in all computing devices.*

# Platinum Founding Members

RISC-V

Berkeley Architecture Research

bluespec

cortus

Hewlett Packard Enterprise

DRAPER

Google

Microsoft

NVIDIA

IBM

Mellanox TECHNOLOGIES

QUALCOMM

WD Western Digital

Microsemi

SiFive

Rambus

Cryptography Research

# Gold, Silver & Auditor Founding Members

AMD

ANDES TECHNOLOGY

antmicro EMBEDDED SYSTEMS

BAE SYSTEMS

ICT

Blockstream

中科院计算所 INSTITUTE OF COMPUTING TECHNOLOGY, CAS

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Esperanto Technologies

ESPRESSIF

GRAY RESEARCH

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IDT

INTRINSIX

ETH zürich

runtime.io

PROCESSOR

MIT CSAIL

ROA LOGIC

LATTICE SEMICONDUCTOR

VectorBlox embedded supercomputing

Sur Technology

Syntacore Custom cores and tools

Technolution

Rumble Development

# RISC-V Foundation Board of Directors

- Krste Asanović, Chairman
  - Professor in the EECS Department at UC Berkeley
- Zvonimir Bandić
  - Senior Director of Next Generation Platform Technologies at Western Digital Corporation
- Charlie Hauck
  - CEO of Bluespec Inc.
- David Patterson
  - Retired Professor Computer Science UC Berkeley
- Jothy Rosenberg
  - Associate Director of the cyber security group at Draper Laboratories
- Frans Sijstermans
  - Vice President Engineering at NVIDIA
- Ted Speers
  - Technical Fellow, Head of Product Architecture for Microsemi's SoC Group

# Bi-annual Workshops

- 1st RISC-V workshop Jan 14-15, 2015 in Monterey, CA
  - Sold out: **144** (33 companies & 14 universities)
  - Slides & videos can be found here
- 2nd RISC-V workshop Jun 29-30, 2015 at UC Berkeley
  - Sold out: **120** (30 companies & 20 universities)
  - Slides & videos can be found here
- 3rd RISC-V workshop Jan 5-6, 2016 at Oracle Redwood City, CA
  - Sold out: **157** (42 companies & 26 universities)
  - Slides & videos can be found here
- 4th RISC-V workshop Jul 12-13, at MIT Cambridge, MA
  - Sold out: **252** (63 companies & 42 universities)
  - Slides & videos can be found here

# RISC-V Workshop #4 at MIT in Cambridge, MA USA

- 252 attendees from 63 companies and 42 universities

# 5th RISC-V Workshop – Save the Date

Nov 29th – 30th, 2016

Google Mountain View, CA


# Foundation Status

- Articles of Incorporation filed August 2015
  - RISC-V Foundation Corporation is a legal, non-profit operating entity
- Signed on 40+ Founding members
  - shaped the initial by-laws and membership agreements
- Board of Directors formed in Q2 of 2016
  - Ratify Membership Agreement
  - Ratify set of Bylaws
- **This is just the beginning of RISC-V...**

# RISC-V Extensions

- None ratified by foundation.
  - But no changes are expected.
- 2.0 means "frozen".
- 1.9 means "almost finished".
  - Aka: "speak now or forever hold your peace."

| Base | Version | Frozen? |
|---|---|---|
| RV32I | 2.0 | Y |
| RV32E | 1.9 | N |
| RV64I | 2.0 | Y |
| RV128I | 1.7 | N |
| **Extension** | **Version** | **Frozen?** |
| M | 2.0 | Y |
| A | 2.0 | Y |
| F | 2.0 | Y |
| D | 2.0 | Y |
| Q | 2.0 | Y |
| L | 0.0 | N |
| C | 1.9 | N |
| V | 0.1 | N |
| B | 0.0 | N |
| T | 0.0 | N |
| P | 0.1 | N |

# Memory Model

- currently very relaxed
  - use fences to enforce desired ordering
- Work in progress to provide a formally verified MM
- Goal is to make implementing the C11/C++11 memory model easy
  - acquire/release on AMOs will match the C standard (but not quite sure how to specify this concisely and exactly)
- At a minimum:
  - we will enforce load-load ordering to the same address within a single thread

# “C”: Compressed Instruction Extension

- C extension adds 2 byte instructions
  - RVC => RVI decoder only ~700 gates (~2% of small core)
- **50%-60% instructions compress -> 25%-30% smaller**
- Finished, but not yet frozen
- Read Andrew's PhD thesis!
  - "Design of the RISC-V ISA"
  - https://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-1.html

# "V": RISC-V Standard Vector Extension

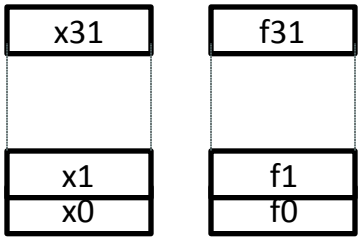
- To be discussed at next RISC-V workshop
  - not quite ready yet
- Efficient and scalable to all reasonable design points
  - Low-cost or high-performance
  - In-order, decoupled, or out-of-order microarchitectures
  - Integer, fixed-point, and/or floating-point data types

- Non-goal: Look like everyone's Packed-SIMD
- Non-goal: Look like a GPU

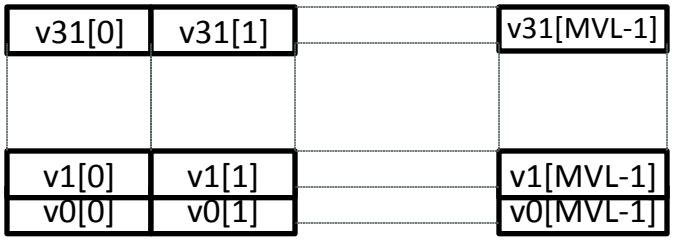
- Read Krste's Thesis:
  - "Vector microprocessors"
  - https://people.eecs.berkeley.edu/~krste/thesis.html

# Proposed V Extension State

Standard RISC-V scalar x and f registers



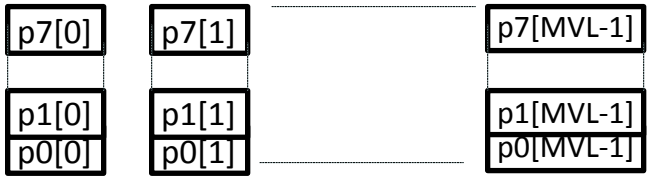

Up to 32 vector data registers, v0-v31, of at least 4 elements each, with variable bits/element (8,16,32,64,128)




MVL is maximum vector length, implementation and configuration dependent, but MVL >= 4

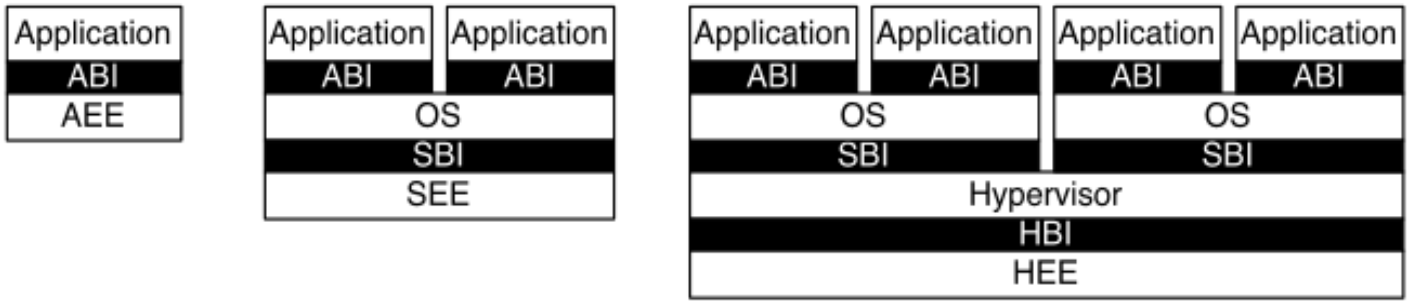
Vector configuration CSR


Vector length CSR


8 vector predicate registers, with 1 bit per element

# Reference Privileged Architecture




- **not frozen**, but many OS ports exist (Linux, FreeBSD, etc.)
- v1.7 in May 2015
- v1.9 in May 2016
  - riscv-tools, QEMU, Linux
- Getting close, but need more driver/OS development against it.
- hypervisor discussion is beginning
  - type 1 and type 2
- Need to define platform spec below.

# RISC-V External Debug Specification

- For debugging software (requires working hardware!)
- https://dev.sifive.com/documentation/risc-v-external-debug-support/
  - Will be pushed back to RISC-V Foundation.
- Effectively an other privilege mode
- can reserve parts of the address space for MMIO for communicating with the core
- No more Berkeley non-standard HTIF (host/target interface) for tethered communications

# External Debug: how does it work?

- Design goal:
  - **simple, cheap** debug support
- Debug Transport Module (DTM) writes to a debug RAM
- DTM interrupts the core
- core (now in D-privilege mode) jumps to and executes code in debug RAM
- maximum flexibility!
  - read/write a register
  - read/write memory
- Currently uses JTAG, but not tied to that

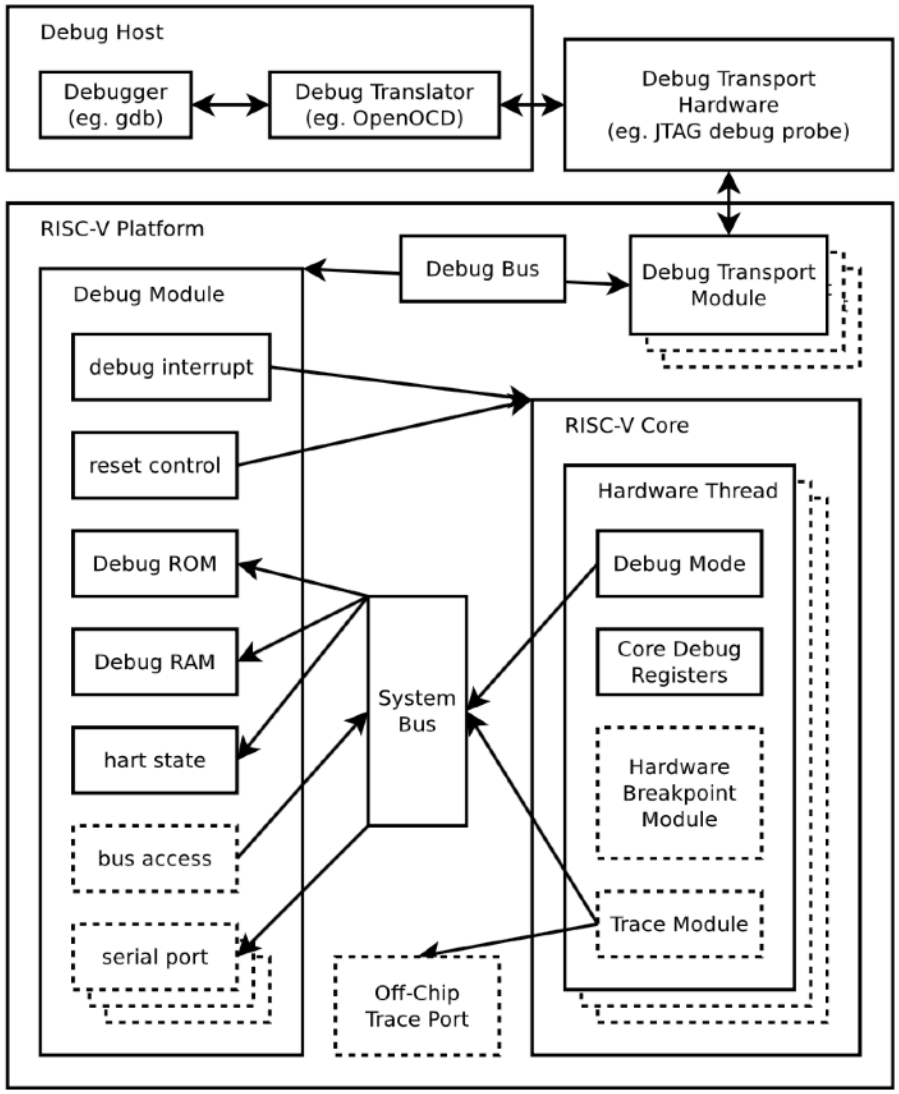
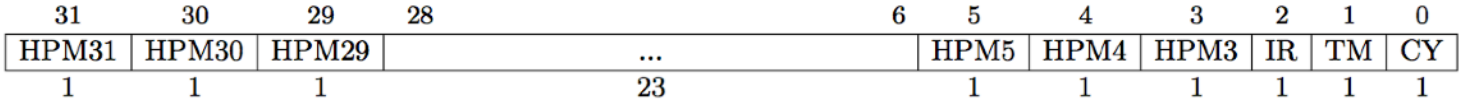



Figure 1: RISC-V Debug System Overview

# High Performance Monitor (HPM) counters

- Goal
  - provide access to micro-architectural events
  - allow software to dynamically choose how to map many events onto a limited set of expensive hardware counters
- Support nearly infinite events
  - branch prediction, cache misses, instruction mixes, mem traffic, etc.
- Support up-to 29 physical hardware counters
  - 29 HPM counters
  - 29 event selectors
  - 3 counter enable registers for [h|s|u] privilege modes.
    - can specify which counters are available to which privilege modes

### 3.1.16 Machine Counter-Enable Registers (m[h|s|u]counteren)




- CPU designer chooses what events to have, and how many HPM counters to build.

# Future Progress

- Berkeley and SiFive are producing incremental proposals to current user and privilege specs
  - we will put those on arXiv
- Foundation has its own working groups
  - more to be announced at the RISC-V workshop

# Software Progress

- binutils, gcc
  - ~~"waiting on lawyers"~~, but should be good to go!
- glibc/Linux
  - will upstream after binutils, etc.
- QEMU
  - ucb-bar/riscv-qemu now has user-mode and system-mode
  - currently upstreaming user-mode
- LLVM
  - upstreaming in progress (ask Alex Bradbury)
- Fedora disk images now available
- coreboot
  - "RISC-V is a first class citizen"
- UEFI
- FreeBSD

# RISC-V Ecosystem
# www.riscv.org

- ***Documentation***
  - User-Level ISA Spec
  - Privileged ISA draft
  - Compressed ISA draft
  - External Debug draft
- ***Software Tools***
  - GCC/glibc/GDB
  - LLVM/Clang
  - Verification Suite
- ***Software***
  - Linux, FreeBSD
  - Yocto
  - Fedora disk images
- ***Software Implementations***
  - QEMU
  - Spike, In-house ISA Sim.
  - ANGEL, JavaScript ISA Sim.
- ***Hardware Implementations***
  - UCB Rocket Chip Generator
    - Rocket in-order core
    - BOOM out-of-order core
  - External implementations
    - PicoRV32
    - Pulp Platform
    - mRISCV
    - and many many more...

# RISC-V Summary

- Strong Industry Support
  - 40+ Founding Sponsors
  - Broad commercial and academic interest (252 workshop attendees representing 63 companies & 42 universities)
- Membership & Bylaw documents being ratified
- Board of Directors formed in Q2 2016
- 5th RISC-V Workshop save the date…

Nov 29th – 30th, 2016
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# Backup Slides

# Foundation Functions

- official source of information about RISC-V, maintains an online repository of RISC-V documents, and promotes adoption of RISC-V by organizing both online and live events
- responsible for sustaining, evolving and open-source licensing of the RISC-V instruction set architecture and surrounding hardware and software ecosystem over time in response to changes in technology and the needs and requests of the user community
- manages licensing of the RISC-V trademarks and provides a vehicle to decide whether a project or product can use the RISC-V trademark
- maintains a directory of public-domain instruction set architecture and micro-architectural techniques, culled from publications and expired patents
- produces and sells RISC-V promotional material, the proceeds from which are used to further the goals of the Foundation

# Foundation Organization

- The Board of Directors consists of seven+ members, whose replacements are elected by the membership
- The Board is ultimately responsible for fulfilling the Mission Statement
- The Board can amend the By-Laws of the RISC-V foundation via a two-thirds affirmative vote
- The Board appoints chairs of ad-hoc committees to address issues concerning RISC-V, and has the final vote of approval of the recommendation of the ad-hoc committees.
- All members of committees must be members of the RISC-V Foundation
  - Committee chairs must report to the Board, and committees are subject to termination if the Board decides a committee is not making satisfactory progress
- Given the worldwide interest in RISC-V, the Board will appoint Chairs of Regional Committees to promote RISC-V development in local communities

# Classes of Membership

- Platinum Sponsor dues of US$25,000 per year
  - 10 complimentary registrations for RISC-V meetings during the year of membership and the most prominent and largest display of company logos in online and print materials for RISC-V
- Platinum members are eligible for Board seat elections and to Chair Foundation Technical Committees, Marketing Committees and Sub-Committees
- Gold Sponsor dues of US$10,000 per year
  - 7 complimentary registrations for RISC-V meetings during the year of membership and prominent display of company logos in online and print materials for RISC-V
- Gold Sponsor members are eligible to Chair Foundation Technical Committees, Marketing Committees and Sub-Committees
- Silver Sponsor dues of US$5,000 per year
  - 5 complimentary registrations for RISC-V meetings and for their logos to be displayed in RISC-V online and print materials
- All Sponsor organizations have one vote per open position in Board elections.
- Auditor dues of US$2,500 per year (non-voting)
  - 2 complimentary registrations for RISC-V meetings during the year of membership and for their names to be listed in online and print materials for RISC-V
- Individual Member dues of US$99 per year (non-voting)

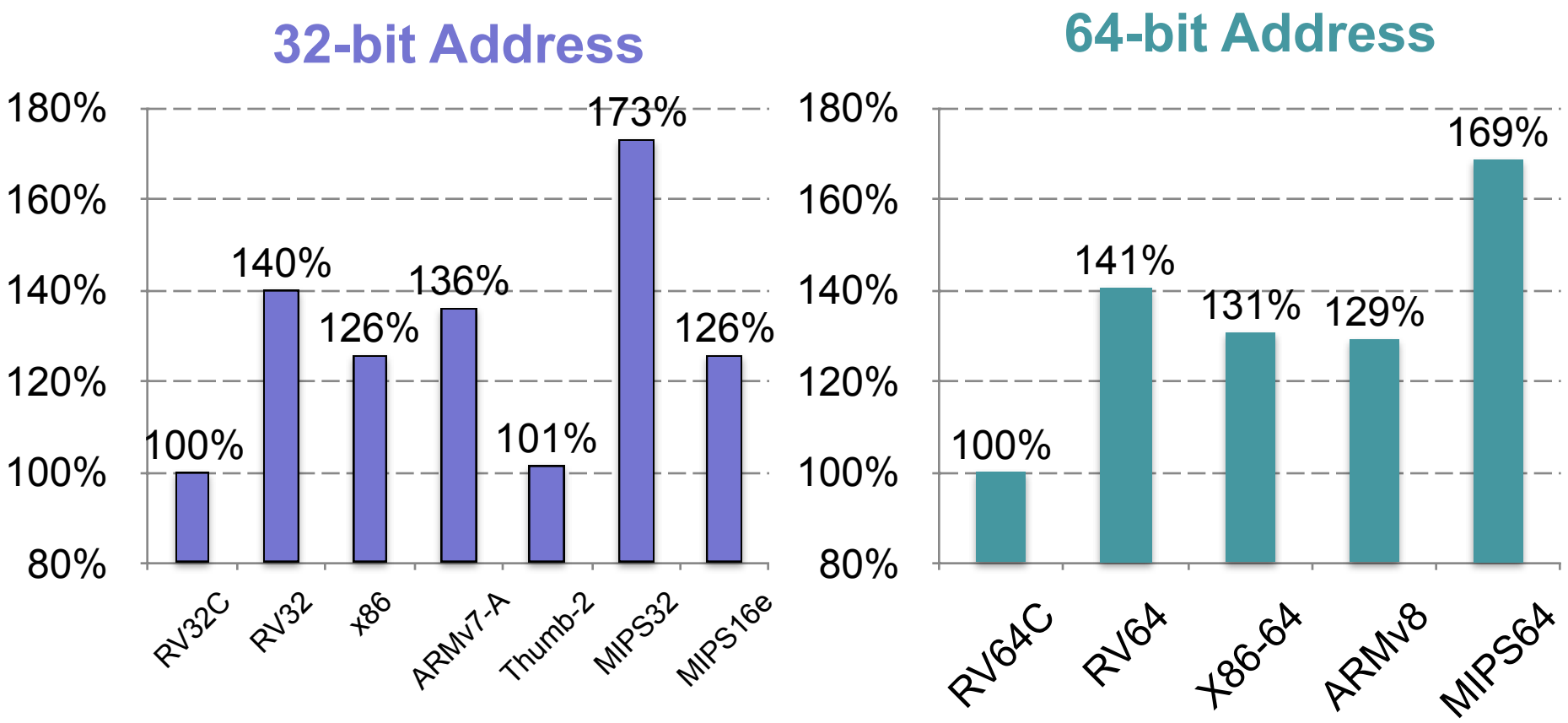
# What's Different about RISC-V?

- ***Simple***
  - Far smaller than other commercial ISAs
- ***Clean-slate design***
  - Clear separation between user and privileged ISA
  - Avoids µarchitecture or technology-dependent features
- A ***modular*** ISA
  - Small standard base ISA
  - Multiple standard extensions
- Designed for ***extensibility/specialization***
  - Variable-length instruction encoding
  - Vast opcode space available for instruction-set extensions
- ***Stable***
  - Base and standard extensions are frozen
  - Additions via optional extensions, not new versions

# SPECint2006 compressed code size

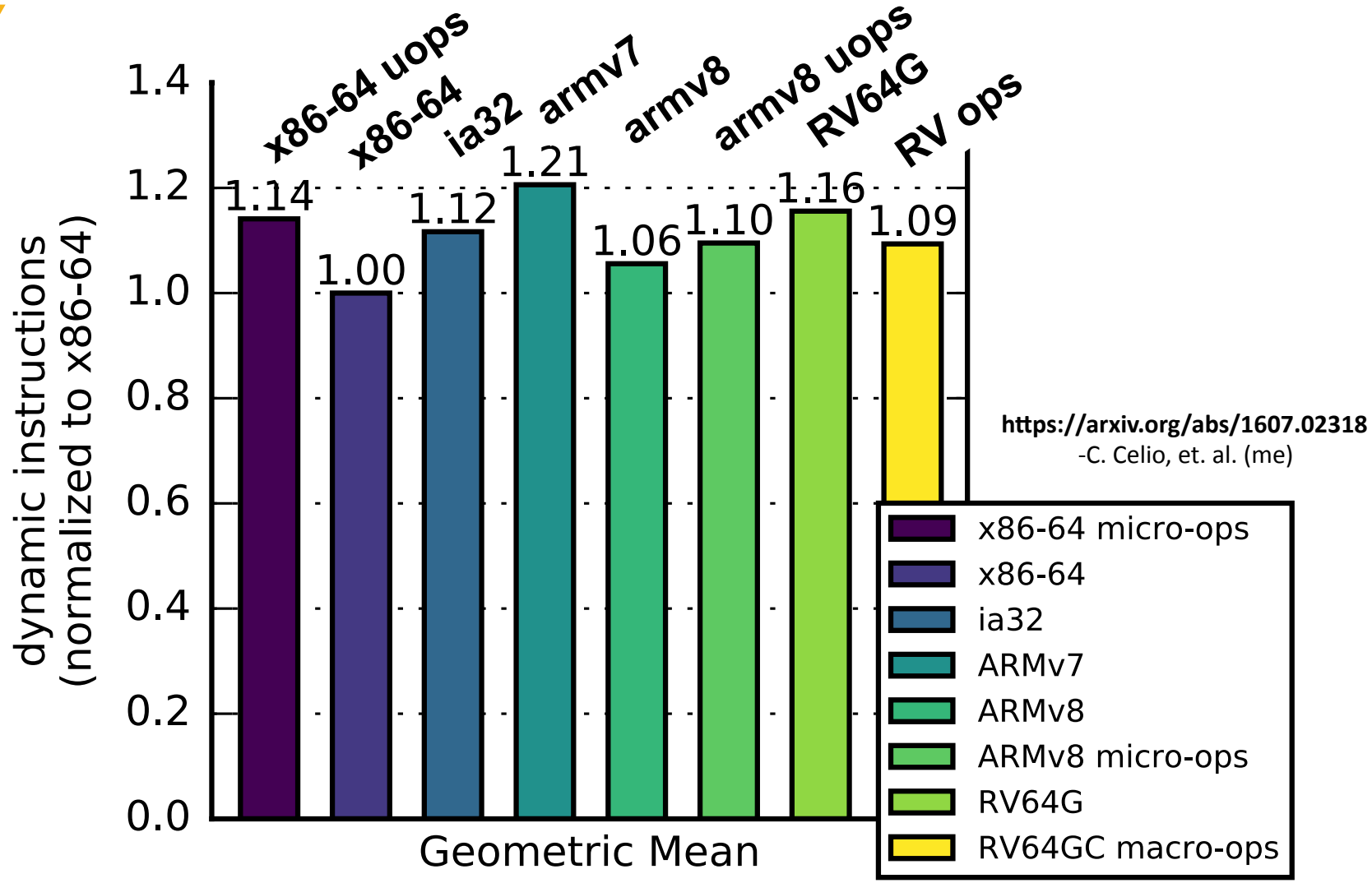
## with save/restore optimization

## (relative to "standard" RVC)




- RISC-V now smallest ISA for 32- and 64-bit addresses

# Dynamic Instructions of SPECInt2006




- RV64GC+macro-op fusion executes **same number** of micro-ops as ARMv8 micro-ops, x86 micro-ops